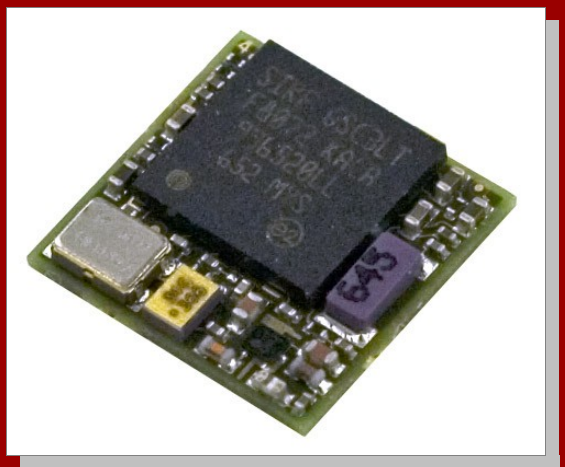
FALCOM
WIRELESS COMMUNICATIONS GMBH

GPS-Receiver

JP18

Application Notes



Version: 1.0.5; Last Modified: 05/05/2009

TABLE OF CONTENTS

VERSION HISTORY:

This table provides a summary of the document revisions.

Version	Author	Changes	Modified
1.0.5	F. Beqiri	- ROM mode removed - No more available. - To run the internal firmware, connect DATA1 to Ground and leave DATA0 open. - Throughout this document the SLC *(SirfLock)* removed.	05/05/2009
1.0.4	F. Beqiri	- In the hardware revision "4d", the ON/OFF pin is internally pulled low through a 47KOhm resistor.	11/02/09
1.0.3	F. Beqiri	- VRTC_REG_IN must be always connected to the VCC pin.	06/06/2008
1.0.2	F. Beqiri	- The firmware version ROM is very early (engineering proof) and was never intended for production use.	23/05/2008
1.0.1	F. Beqiri	- Changed input voltage range of **VRTC_REG_IN** and **VCC** from **3.4 .. 5.5** to **3.3 .. 5.5 V**. - Replaced EVAL-schematic by a new one.	12/09/2007
1.0.0	F. Beqiri	- Initial version	14/05/2007

1 INTRODUCTION

This application note comprises a brief description of the operation of the FALCOM JP18, pad design and layout, design of the solder-mask, and an application circuit.

1.1 General

The JP18 GPS receiver can operate either from internal ROM or internal FLASH.

Important: *The firmware version ROM is very early (engineering proof) and was never intended for production use.*

1.2 Technical data (briefly)

- ***FLASH:***
  - ✔ *Output NMEA messages.*
    - ✔ *Baudrate: 38400 bps,*
    - ✔ *RMC, GGA, GSA, GSV - (1 x 1 sec.)*
- ***BOOTMODE:***
  - ✔ *To load a new firmware into the internal FLASH use SiRFflash tool version 3.2 or higher .*

1.3 ROM and Flash Memory Operating Modes

A combination between **DATA 0** and **DATA 1** pins allows you a choice between operating from ROM or FLASH memory.

	DATA 0	**DATA 1**
No-operation	Open	Open
FLASH	Open	Connect to GND
BOOTMODE	Connect to VIO	Open

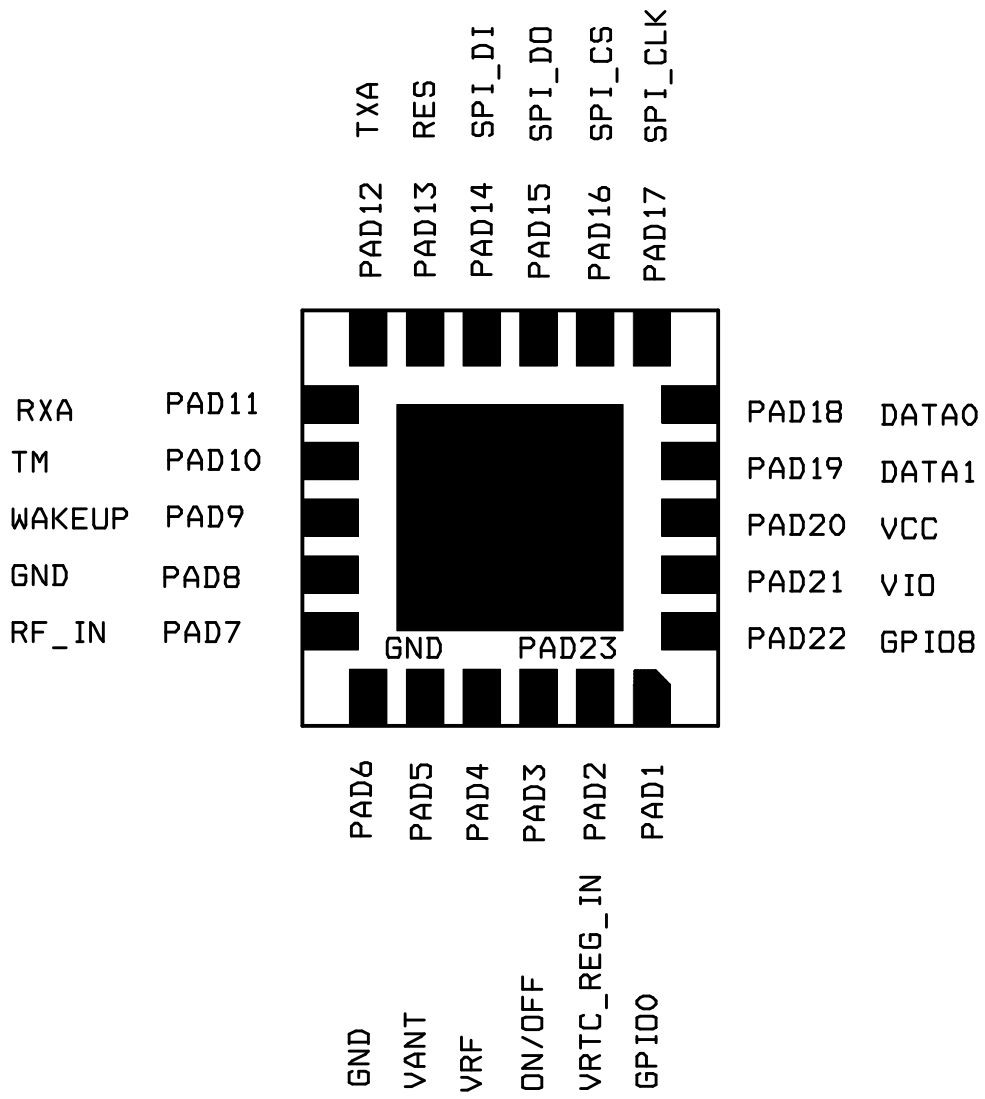
Table 1: ROM and Flash Memory Operating Modes

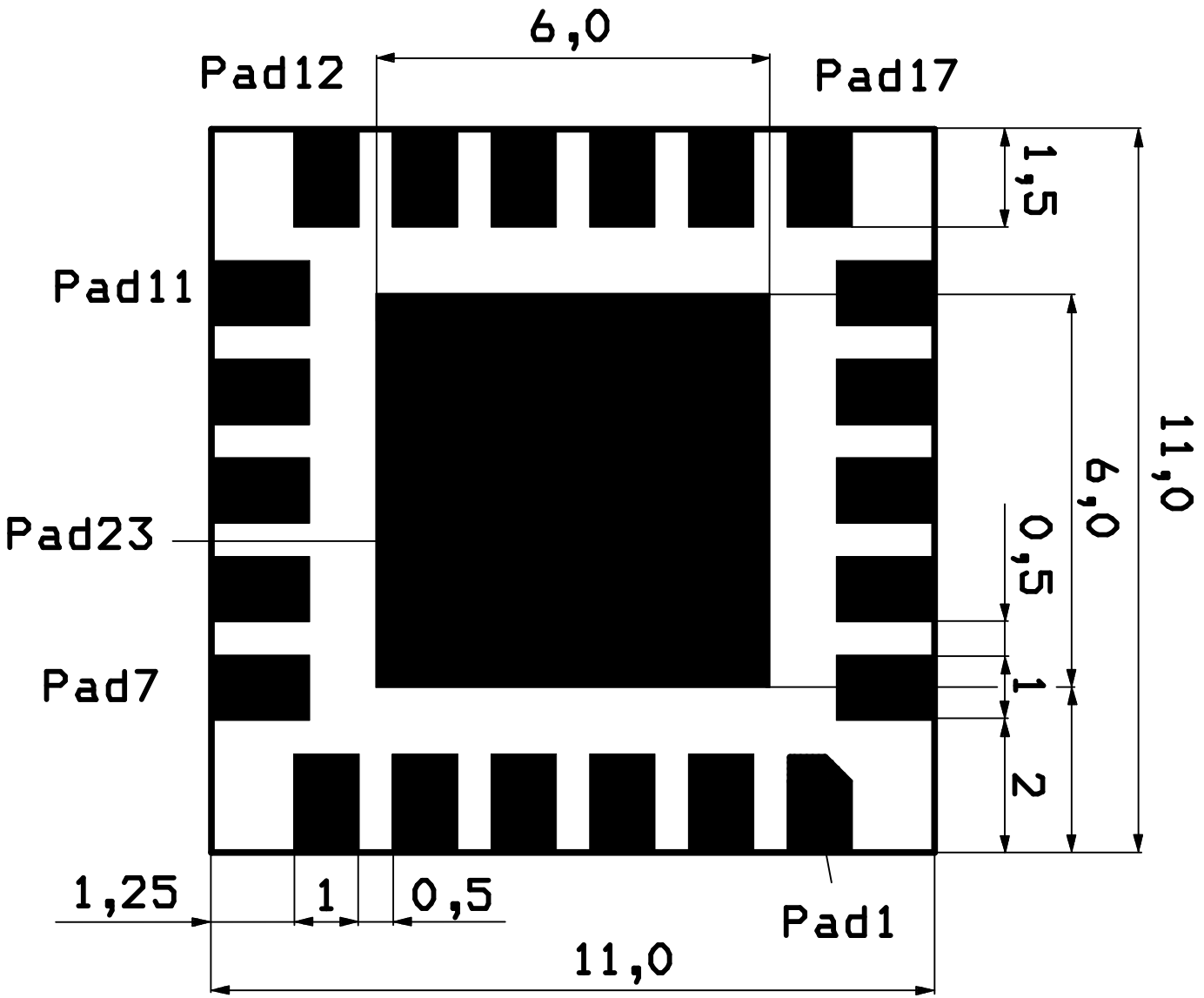
1.4 Pad description and signal levels

Pad	Description	Level	Function
1	GPIO 0	1.8 V	Input/Output
2	VRTC_REG_IN	3.3 V – 5.5 V	Input. *It must be always connected to the VCC pin.*
3	ON/OFF*	1.2 V	Input. In the hardware revision "4d", this pin is pulled low through a 47KOhm resistor. If not used leave it open.
4	VRF	2.7 V	Output
5	VANT	2.7 V – 5 V	Input
6	GND	0 V	-
7	RF_IN	50 Ohms @ 1.575 GHz	Input
8	GND	0 V	-
9	WAKEUP	1.2 V	Output
10	TM	1.8 V	Output
11	RXA	1.8 V	Input
12	TXA	1.8 V	Output
13	RES	1.2 V	Input
14	SPI_DI	1.8 V	Input
15	SPI_DO	1.8 V	Output
16	SPI_CS	1.8 V	Input
17	SPI_CLK	1.8 V	Input
18	DATA 0	1.8 V	Input at startup
19	DATA 1	1.8 V	Input at startup
20	VCC	3.3 V – 5.5 V	Input
21	VIO	1.8 V	Output
22	GPIO 8	1.8 V	Input/Output

* ***F****or more technical details regarding the ON/OFF pin, please refer to the "JP18_hardware_manual.pdf" manual , chapter* ***6.2****.*

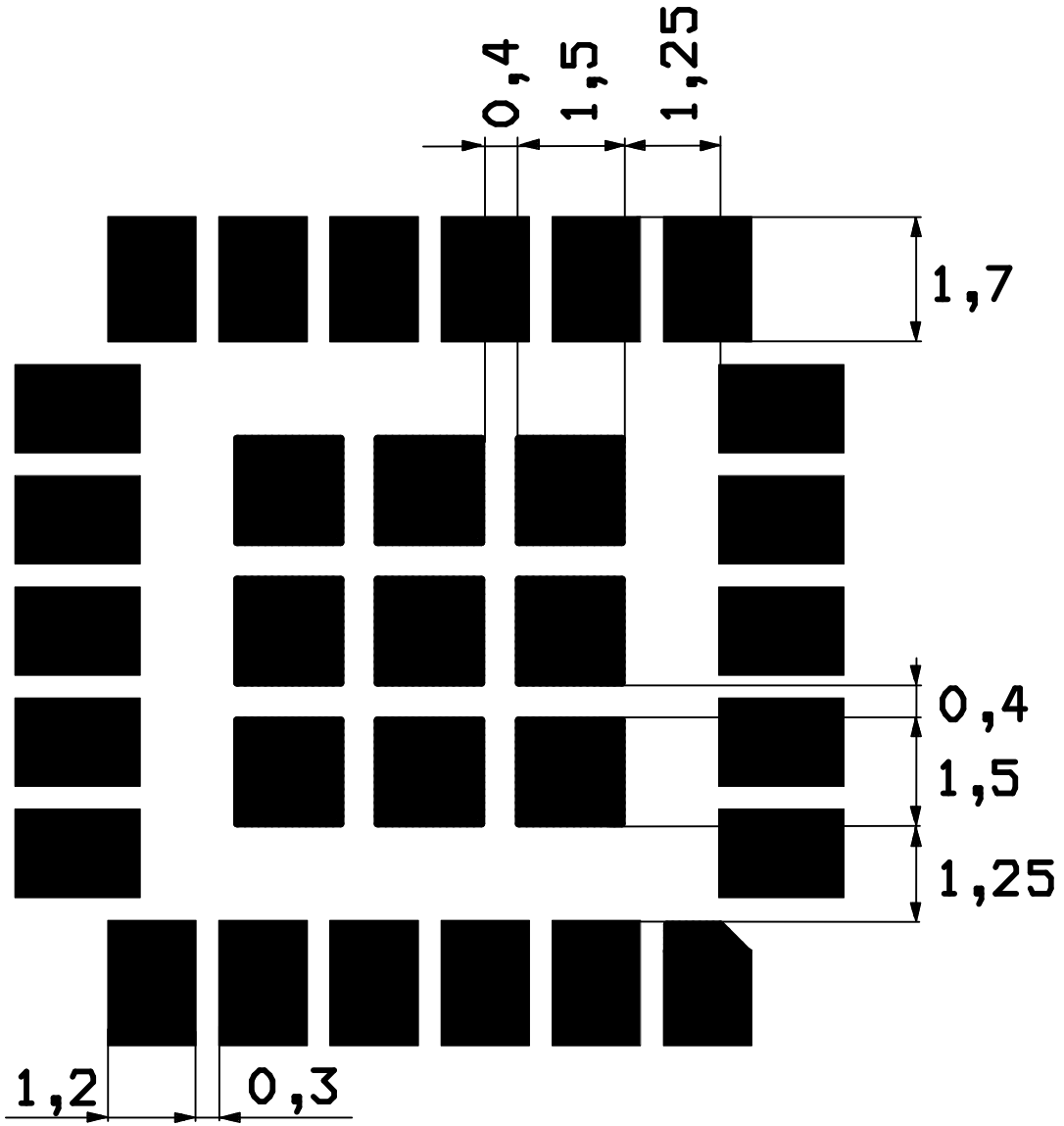
Table 2: Pin description and signal levels


TXA
RES
SPI_DI
SPI_DO
SPI_CS
SPI_CLK
PAD12
PAD13
PAD14
PAD15
PAD16
PAD17
RXA
PAD11
TM
PAD10
WAKEUP
PAD9
GND
PAD8
RF_IN
PAD7
PAD18
DATA0
PAD19
DATA1
PAD20
VCC
PAD21
VIO
PAD22
GPIO8
GND
PAD23
PAD6
PAD5
PAD4
PAD3
PAD2
PAD1
GND
VANT
VRF
ON/OFF
VRTC_REG_IN
GPIO0



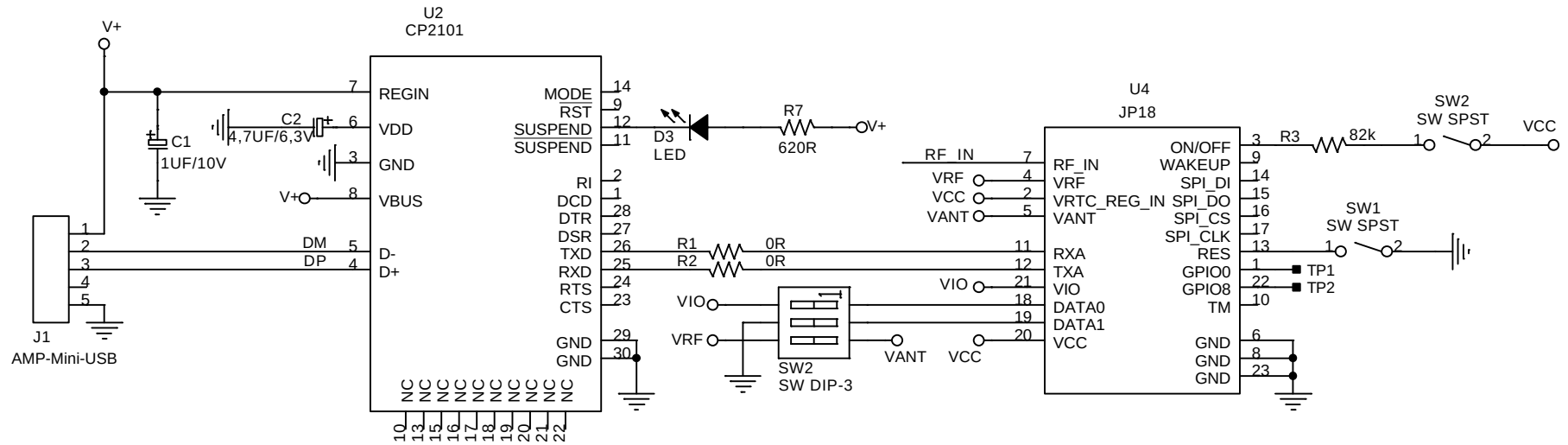
UNIT: mm

Bottom View

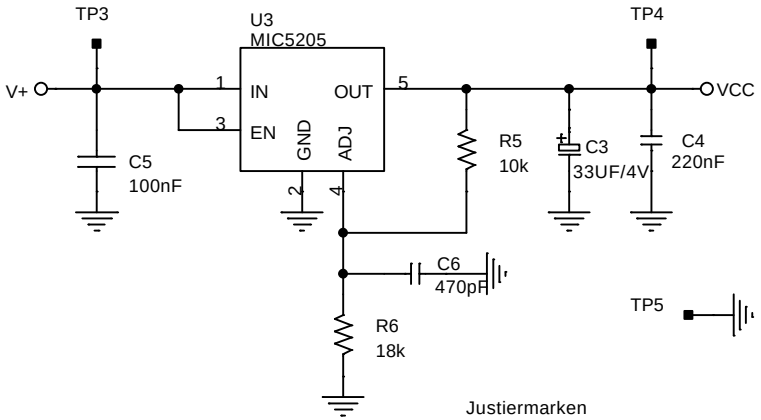


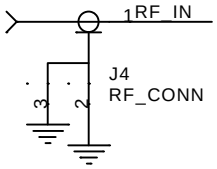
UNIT: mm

Soldermask: Bottom View



	Switch at Data0	Switch at Data1
No-operation	open	open
run from Flash	open	connect to GND
Bootmode	connect to VIO	open





Note: The dimensions of R3/R4 are for VCC=3.3V

ON/OFF-Level is 1.2V!

Justiermarken

JUST1

JUST2

FALCOM

Gewerbering 6

98704 Langewiesen

Title: JP18 - Application-Circuitry

Size: A | Document Number | Rev: 01b

Date: Wednesday, September 12, 2007 | Sheet 1 of 1